# IN THE UNITED STATES DISTRICT COURT FOR THE WESTERN DISTRICT OF TEXAS WACO DIVISION

**BURLEY LICENSING LLC,** 

Plaintiff,

Civil Action No. 6:22-cv-01033

v.

Jury Trial Demanded

ASUSTEK COMPUTER INC.,

Defendant.

## COMPLAINT FOR PATENT INFRINGEMENT

Plaintiff Burley Licensing LLC ("Burley") files this Complaint against ASUSTek
Computer Inc. (referred to herein as "ASUS" or "Defendant") for patent infringement of
United States Patent No. 7,082,167 (the "patent-in-suit") and alleges as follows:

# **NATURE OF THE ACTION**

1. This is an action for patent infringement arising under the patent laws of the United States, 35 U.S.C. §§ 1 *et seq.* 

#### THE PARTIES

- 2. Plaintiff Burley Licensing LLC is a Texas limited liability company with a principal place of business located at 4757 W. Park Blvd, Suite 113-1097, Plano, Texas 75093.
- 3. On information and belief, Defendant ASUSTek Computer Inc. is a corporation organized and existing under the laws of Taiwan that maintains an established place of business at No. 15, Li-Te Road, Beitou District, Taipei City 112, Taiwan.
- 4. On information and belief, ASUS infringes the patent-in-suit by at least making, selling, offering for sale, and/or importing, without authorization, Burley's proprietary technologies as contained in a number of its commercial products including, *inter alia*, laptops and other computer hardware branded with the ASUS trademark; laptops and computer hardware incorporating Graphics Processing Units (GPUs) incorporating the NVENC¹ video encoding feature; laptops and computer hardware incorporating GeForce 600 series GPUs; laptops and computer hardware incorporating GeForce 700 series GPUs; laptops and computer hardware incorporating GeForce 10 series GPUs; laptops and computer hardware incorporating GeForce 16 series GPUs; laptops and computer hardware incorporating GeForce 20 series GPUs; laptops and computer hardware incorporating GeForce 20 series GPUs; laptops and computer hardware incorporating GeForce 20 series GPUs; laptops and computer hardware incorporating GeForce 20 series GPUs; laptops and computer hardware incorporating GeForce 20 series GPUs; laptops and computer hardware incorporating GeForce 20 series GPUs; laptops and computer hardware incorporating GeForce 20 series GPUs; laptops and computer

<sup>&</sup>lt;sup>1</sup> See https://en.wikipedia.org/wiki/Nvidia\_NVENC.

hardware incorporating the NVIDIA GeForce GTX 1050 GPU; laptops and computer hardware incorporating the NVIDIA GeForce GTX 1060 GPU; model ROG Zephyrus laptops; <sup>2</sup> model ROG Flow laptops; <sup>3</sup> model ROG Strix laptops; <sup>4</sup> model TUF Gaming laptops model; <sup>5</sup> model TUF Dash laptops model; <sup>6</sup> ASUS ROG Strix GT Gaming Desktop models; <sup>7</sup> ASUS ROG Strix GA Gaming Desktop models; <sup>8</sup> ASUS ROG Strix series graphics cards; <sup>9</sup> ASUS ROG Matrix series graphics cards; <sup>10</sup> ASUS Dual series graphics cards; <sup>11</sup> ASUS TUF Gaming series graphics cards; <sup>12</sup> ASUS Turbo series graphics cards; <sup>13</sup>

<sup>&</sup>lt;sup>2</sup> See e.g., https://www.asus.com/us/Laptops/For-Gaming/All-series/filter?SubSeries=ROG-Zephyrus.

<sup>&</sup>lt;sup>3</sup> See e.g., https://rog.asus.com/us/laptops/rog-flow/rog-flow-z13-2022-series/.

<sup>&</sup>lt;sup>4</sup> See e.g., https://rog.asus.com/us/laptops/rog-strix/rog-strix-scar-17-se-2022-series/

<sup>&</sup>lt;sup>5</sup> See e.g., https://www.asus.com/us/Laptops/For-Gaming/TUF-Gaming/ASUS-TUF-Gaming-A15-2022/

<sup>&</sup>lt;sup>6</sup> See e.g., https://www.asus.com/us/Laptops/For-Gaming/TUF-Gaming/ASUS-TUF-Dash-F15-2022/.

<sup>&</sup>lt;sup>7</sup> See e.g., https://www.asus.com/us/site/gaming/rog/gaming-desktops/strix-gt.html.

<sup>&</sup>lt;sup>8</sup> See e.g., https://www.asus.com/us/site/gaming/rog/gaming-desktops/strix-ga.html

<sup>&</sup>lt;sup>9</sup> See e.g., https://rog.asus.com/us/graphics-cards/graphics-cards/rog-strix/rog-strix-rtx3090-o24g-eva-model/.

 $<sup>^{10}</sup>$  See e.g., https://rog.asus.com/us/graphics-cards/graphics-cards/rog-matrix/rog-matrix-rtx2080ti-p11g-gaming-model/.

<sup>&</sup>lt;sup>11</sup> See e.g., https://www.asus.com/us/Motherboards-Components/Graphics-Cards/Allseries/filter?Category=NVIDIA&Series=Dual&Spec=625./

<sup>&</sup>lt;sup>12</sup> See e.g., https://www.asus.com/us/Motherboards-Components/Graphics-Cards/Allseries/filter?Category=NVIDIA&Series=TUF-Gaming&Spec=625.

<sup>&</sup>lt;sup>13</sup> See e.g., https://www.asus.com/us/Motherboards-Components/Graphics-Cards/Allseries/filter?Category=NVIDIA&Series=Turbo&Spec=625.

ASUS Phoenix series graphics cards;<sup>14</sup> ASUS KO series graphics cards;<sup>15</sup> and other laptops and computer hardware which function in a substantially similar way to the previously specified laptops and computer hardware. (Collectively and individually referred to herein as the "Accused Computer Products.")

### **JURISDICTION AND VENUE**

- 5. This Court has subject matter jurisdiction over this action pursuant to 28 U.S.C. §§ 1331 and 1338(a) because this action arises under the patent laws of the United States, 35 U.S.C. §§ 1 et seq.
- 6. ASUS is subject to personal jurisdiction in the United States, and specifically in Texas, pursuant to Fed. R. Civ. P. 4(k)(2). On information and belief, ASUS is not subject to jurisdiction in any state's courts of general jurisdiction. ASUS has sufficient minimum contacts with the United States that include, *inter alia*, importing, advertising, offering to sell, and/or selling the Accused Computer Products throughout the United States, including in the State of Texas and this judicial district, and such that ASUS should reasonably and fairly anticipate being hauled into court in the State of Texas and this judicial district.
- 7. This Court has personal jurisdiction over ASUS pursuant to the Texas Long Arm Statute. See Tex. Civ. Prac. & Rem. Code §§ 17.042(1), (2), and (3).

<sup>&</sup>lt;sup>14</sup> See e.g., https://www.asus.com/us/Motherboards-Components/Graphics-Cards/Allseries/filter?Category=NVIDIA&Series=Phoenix&Spec=625.

<sup>&</sup>lt;sup>15</sup> See e.g., https://www.asus.com/us/Motherboards-Components/Graphics-Cards/Allseries/filter?Category=NVIDIA&Series=KO&Spec=625.

- 8. On information and belief, ASUS is subject to the Court's personal jurisdiction because it regularly conducts and solicits business, or otherwise engages in other persistent courses of conduct in the State of Texas and in this judicial district, and/or derives substantial revenue from the importation, sale, and distribution of goods and services, including but not limited to the Accused Computer Products, to individuals and businesses in the State of Texas and in the Western District of Texas.
- 9. On information and belief, ASUS has purposefully directed its marketing, sales, distribution, and importation activities towards, and in relation to, the State of Texas and its residents.<sup>16</sup>
- 10. On information and belief, ASUS has delivered the Accused Computer Products into the stream of commerce with the expectation that they will be purchased by consumers residing in the State of Texas and in the Western District of Texas.
- 11. This Court has personal jurisdiction over ASUS because, inter alia, ASUS, on information and belief: (1) has committed acts of patent infringement in this State and judicial district, (2) has substantial, continuous, and systematic contacts with this State and this judicial district; (3) enjoys substantial income from its operations and sales in this State and this judicial district; and (4) solicits business and markets products, systems and/or services in this State and judicial district including, without limitation, related to the Accused Computer Products.

<sup>&</sup>lt;sup>16</sup> See e.g., http://promos.asus.com/US/where to buy/

12. Venue is proper pursuant to 28 U.S.C. §§ 1391(c) because ASUS is a foreign corporation not residing in a United States judicial district, and, therefore, they may be sued in any judicial district pursuant to 28 U.S.C. §§ 1391(c)(3).

### United States Patent No. 7,082,167

- 13. On July 25, 2006, the United States Patent and Trademark Office ("USPTO") duly and legally issued United States Patent No. 7,082,167 ("the '167 patent") entitled "Method and Device for Controlling the Quality of Video Data" to inventors Patrice Alexandre, Xavier Ducloux, and Gildas Guelou.
  - 14. The '167 patent is presumed valid under 35 U.S.C. § 282.
  - 15. Burley owns all rights, title, and interest in the '167 patent.
- 16. Burley has not granted ASUS an approval, an authorization, or a license to the rights under the '167 patent.
- 17. The '167 patent relates to, among other things, video encoding technology on computer video cards, also known as graphic processing units (GPUs), and multipass video encoding.
- 18. The claimed invention(s) of the '167 patent sought to solve problems with, and improve upon, existing video encoding technologies. For example, the '167 patent states:

Video compression according to certain standards, and especially according to the MPEG2 standard, is known as a method of "non-transparent coding which, in particular, makes it possible to represent a video-data sequence in the form of a stream of binary elements the throughput of which is adjustable to the conditions of storage and/or of transport of the stream. The terminology "non-transparent' means that the coding algorithms used adapt the level of degradation applied to the data sequence as a function of the entropy level of the

video signal and of the desired throughput for the resulting stream. The degradations applied are the result of a process of quantization of coefficients representative of the video signal after DCT (Discrete Cosine Transform) transformation.

For a binary stream of constant throughput, the method of coding according to the MPEG2 standard permanently adjusts the quantization level of the DCT coefficients in such a way that their coding generates a binary stream in accordance with the target bitrate. Such an approach tends to make the level of degradation variable, for a video signal the entropy of which varies over time. Hence, fixed-throughput coding generates a variable level of coding quality.

When several video sequences are transported jointly on a transmission channel with fixed bandwidth (as in the case of a satellite transponder, for example), it is preferable to share the usable throughput between the coding methods via a centralized throughput-allocation algorithm. This solution, widely presented under the title of statistical multiplexing, makes it possible to reduce the overall degradation perceived by 10 to 30% on average by comparison with sharing in a mode with fixed throughput for each video sequence.

More particularly, the statistical multiplexing applies a reduction in the dispersion of coding quality between the video sequences, by distributing more throughput to the video sequences exhibiting the greatest entropy.

Nevertheless, statistical multiplexing is based on the statistical properties of the content of video sequences in finite numbers, such that the coding quality perceived in the course of time still exhibits fluctuations. For example, when all the video sequences simultaneously exhibit very high entropy, the overall quality of the coding becomes less than the average service quality. Conversely, when video sequences of low entropy are transmitted at the same instant, the overall quality of the coding then becomes higher than the average coding quality.

In this latter case, it becomes advantageous to reduce the total throughput allocated to the coding of the video sequences in favour of the data of an opportunistic nature (data the throughput of which is not guaranteed). The coding of each video sequence then takes place by limiting its throughput to that making it possible to obtain the quality of service envisaged.

See '167 Specification at col. 1, ll. 12-63.

#### 19. The '167 patent then states:

However, in order to obtain an effective method of sharing bandwidth while guaranteeing a level of quality for all the video sequences, it is important to take into account the content of the video sequences. This is because the quantity of information necessary to code a video sequence depends on the entropy of these sequences. The higher the entropy, the greater the quantity of information necessary to code it in order to guarantee a constant quality, and, conversely, the lower the entropy, the lower the quantity of information.

The invention thus proposes to guarantee a constant quality of the video data after decoding, taking into account the spatial and/or time-domain complexity of the data in order to determine the quantization interval.

See '167 Specification at col. 2, ll. 9-21.

### 20. The '167 patent then states:

One of the particular features of the invention is the definition of a parametric quality model via which the user is in a position to define the desired quality of service, the parametric model proposed taking into account criteria for appreciating the quality subjectively perceived after coding. This is because the methods of coding by quantization of the DCT coefficients exhibit the difficulty of not giving a constant subjective perception of quality for a given level of quantization. More precisely, the data sequences featuring low richness of content (e.g.: large plane on a face), for equivalent subjective quality rendition, require a lower level of quantization than for sequences the content of which features high richness (e.g., crowd of a football stadium).

The benefit of the invention is that of taking into consideration the abovementioned characteristics in a parametric quality model in which the level of spatial-temporal complexity of the video sequence to be coded plays a part as an element for adjusting the average quantization level envisaged.

See '167 Specification at col. 2, ll. 43-61.

21. The invention(s) claimed in the '167 patent solves various technological problems inherent in the then-existing video encoding systems and enables such systems to, among other things, maintain constant quality of video stream while effectively mitigating bandwidth usage.

#### **CLAIMS FOR RELIEF**

### Count I - Infringement of United States Patent No. 7,082,167

- 22. Burley repeats, realleges, and incorporates by reference, as if fully set forth here, the allegations of the preceding paragraphs above.
- 23. On information and belief, ASUS (or those acting on its behalf) makes, uses, sells, offers to sell, and/or imports the Accused Computer Products, which infringe (literally and/or under the doctrine of equivalents) at least claim 1 of the '167 patent.
- 24. On information and belief, the Accused Computer Products conform to the requirements of the NVIDIA NVENC API Program Guide.
- 25. On information and belief, the Accused Computer Products employ and provide a method of monitoring the quality of video data having to undergo coding and decoding, making it possible to maintain predetermined constant quality of the video data after decoding, as demonstrated below.

NVENC supports several rate control modes and provides control over various parameters related to the rate control algorithm via structure NV\_ENC\_INITIALIZE\_PARAMS::encodeConfig::rcParams. The rate control algorithm is implemented in NVENC firmware.

NVENC supports the following rate control modes:

Constant bitrate (CBR): Constant bitrate is specified by setting rateControlMode to NV\_ENC\_PARAMS\_RC\_CBR. In this mode, only averageBitRate is required and used as the target output bitrate by the rate control algorithm. Clients can control the ratio of I to P frames using NV\_ENC\_RC\_PARAMS::lowDelayKeyFrameScale which is useful to avoid channel congestion in case I frame ends up generating high number of bits. Set NV\_ENC\_CONFIG\_H264/NV\_ENC\_CONFIG\_HEVC::enableFillerDataInsertion = 1 incase the bitrate needs to be strictly adhered to.

Variable bitrate (VBR): Variable bitrate is specified by setting rateControlMode to NV\_ENC\_PARAMS\_RC\_VBR. The encoder tries to conform to average bitrate of averageBitRate over the long term while not exceeding maxBitRate any time during the encoding. In this mode, averageBitRate must be specified. If maxBitRate isn't specified, NVENC will set it to an internally determined default value. It is recommended that the client specify both parameters maxBitRate and averageBitRate for better control.

Constant QP: This mode is specified by setting rateControlMode to NV\_ENC\_PARAMS\_RC\_CONSTQP. In this mode, the entire frame is encoded using QP specified in NV\_ENC\_RC\_PARAMS::constQP.

Target quality: This mode is specified by setting rateControlMode to VBR and desired target quality in targetQuality. The range of this target quality is 0 to 51(fractional values are also supported in Video Codec SDK 8.0 and above). In this mode, the encoder tries to maintain constant quality for each frame, by allowing the bitrate to vary subject to the bitrate parameter specified in maxBitRate. The resulting average bitrate can, therefore, vary significantly depending on the video content being encoded. If maxBitRate is not specified, the encoder will use as many bits as needed to achieve the target quality. However, if maxBitRate is set, it will form an upper bound on the actual bitrate. If maxBitRate is set too low in this mode, the bitrate may become constrained, resulting in the desired target quality possibly not being achieved.

See https://docs.nvidia.com/video-technologies/video-codec-

When determining the QP to use for encoding a frame, it is beneficial if NVENC knows the overall complexity of the frame to distribute the available bit budget in the most optimal manner. In some situations, multi-pass encoding may also help catch larger motion between frames. For this purpose, NVENC supports the following types of multi-pass frame encoding modes:

- 1-pass per frame encoding (NV\_ENC\_MULTI\_PASS\_DISABLED)
- 2-passes per frame, with first pass in quarter resolution and second pass in full resolution [NV ENC TWO PASS QUARTER RESOLUTION]
- 2-passes per frame, with both passes in full resolution (NV ENC TWO PASS FULL RESOLUTION).

In 1-pass rate control modes, NVENC estimates the required QP for the macroblock and immediately encodes the macroblock. In 2-pass rate control modes, NVENC estimates the complexity of the frame to be encoded and determines bit distribution across the frame in the first pass. In the second pass, NVENC encodes macroblocks in the frame using the distribution determined in the first pass. As a result, with 2-pass rate control modes, NVENC can distribute the bits more optimally within the frame and can reach closer to the

target bitrate, especially for CBR encoding. Note, however, that everything else being the same, performance of 2-pass rate control mode is lower than that of 1-pass rate control mode. The client application should choose an appropriate multi-pass rate control mode after evaluating various modes, as each of the modes has its own advantages and disadvantages.

NV\_ENC\_TWO\_PASS\_FULL\_RESOLUTION generates better statistics for the second pass, whereas NV\_ENC\_TWO\_PASS\_QUARTER\_RESOLUTION results in larger motion vectors being caught and fed as hints to second pass.

See https://docs.nvidia.com/video-technologies/video-codec-sdk/pdf/NVENC\_VideoEncoder\_API\_ProgGuide.pdf at pp. 10-11.

26. On information and belief, the Accused Computer Products employ and provide a method comprising the step of receiving from at least one coder information representing the complexity of video data to be coded, as demonstrated below.

NVENC supports several rate control modes and provides control over various parameters related to the rate control algorithm via structure NV\_ENC\_INITIALIZE\_PARAMS::encodeConfig::rcParams. The rate control algorithm is implemented in NVENC firmware.

NVENC supports the following rate control modes:

Constant bitrate (CBR): Constant bitrate is specified by setting rateControlMode to NV\_ENC\_PARAMS\_RC\_CBR. In this mode, only averageBitRate is required and used as the target output bitrate by the rate control algorithm. Clients can control the ratio of I to P frames using NV\_ENC\_RC\_PARAMS::lowDelayKeyFrameScale which is useful to avoid channel congestion in case I frame ends up generating high number of bits. Set NV\_ENC\_CONFIG\_H264/NV\_ENC\_CONFIG\_HEVC::enableFillerDataInsertion = 1 incase the bitrate needs to be strictly adhered to.

Variable bitrate (VBR): Variable bitrate is specified by setting rateControlMode to NV\_ENC\_PARAMS\_RC\_VBR. The encoder tries to conform to average bitrate of averageBitRate over the long term while not exceeding maxBitRate any time during the encoding. In this mode, averageBitRate must be specified. If maxBitRate isn't specified, NVENC will set it to an internally determined default value. It is recommended that the client specify both parameters maxBitRate and averageBitRate for better control.

Constant QP: This mode is specified by setting rateControlMode to NV\_ENC\_PARAMS\_RC\_CONSTQP. In this mode, the entire frame is encoded using QP specified in NV\_ENC\_RC\_PARAMS::constQP.

Target quality: This mode is specified by setting rateControlMode to VBR and desired target quality in targetQuality. The range of this target quality is 0 to 51(fractional values are also supported in Video Codec SDK 8.0 and above). In this mode, the encoder tries to maintain constant quality for each frame, by allowing the bitrate to vary subject to the bitrate parameter specified in maxBitRate. The resulting average bitrate can, therefore, vary significantly depending on the video content being encoded. If maxBitRate is not specified, the encoder will use as many bits as needed to achieve the target quality. However, if maxBitRate is set, it will form an upper bound on the actual bitrate. If maxBitRate is set too low in this mode, the bitrate may become constrained, resulting in the desired target quality possibly not being achieved.

See https://docs.nvidia.com/video-technologies/video-codec-

When determining the QP to use for encoding a frame, it is beneficial if NVENC knows the overall complexity of the frame to distribute the available bit budget in the most optimal manner. In some situations, multi-pass encoding may also help catch larger motion between frames. For this purpose, NVENC supports the following types of multi-pass frame encoding modes:

- 1-pass per frame encoding (NV\_ENC\_MULTI\_PASS\_DISABLED)
- 2-passes per frame, with first pass in quarter resolution and second pass in full resolution [NV ENC TWO PASS QUARTER RESOLUTION]
- 2-passes per frame, with both passes in full resolution (NV ENC TWO PASS FULL RESOLUTION).

In 1-pass rate control modes, NVENC estimates the required QP for the macroblock and immediately encodes the macroblock. In 2-pass rate control modes, NVENC estimates the complexity of the frame to be encoded and determines bit distribution across the frame in the first pass. In the second pass, NVENC encodes macroblocks in the frame using the distribution determined in the first pass. As a result, with 2-pass rate control modes, NVENC can distribute the bits more optimally within the frame and can reach closer to the

target bitrate, especially for CBR encoding. Note, however, that everything else being the same, performance of 2-pass rate control mode is lower than that of 1-pass rate control mode. The client application should choose an appropriate multi-pass rate control mode after evaluating various modes, as each of the modes has its own advantages and disadvantages. NV\_ENC\_TWO\_PASS\_FULL\_RESOLUTION generates better statistics for the second pass, whereas NV\_ENC\_TWO\_PASS\_QUARTER\_RESOLUTION results in larger motion vectors being caught and fed as hints to second pass.

See https://docs.nvidia.com/video-technologies/video-codec-sdk/pdf/NVENC\_VideoEncoder\_API\_ProgGuide.pdf at pp. 10-11.

27. On information and belief, the Accused Computer Products employ and provide a method comprising the step of calculating, as a function of the complexity for each video-data item to be coded and of a programmed target quality value for dynamically adjusting the rate to the content, a reference quantization value, as demonstrated below.

NVENC supports several rate control modes and provides control over various parameters related to the rate control algorithm via structure NV\_ENC\_INITIALIZE\_PARAMS::encodeConfig::rcParams. The rate control algorithm is implemented in NVENC firmware.

NVENC supports the following rate control modes:

Constant bitrate (CBR): Constant bitrate is specified by setting rateControlMode to NV\_ENC\_PARAMS\_RC\_CBR. In this mode, only averageBitRate is required and used as the target output bitrate by the rate control algorithm. Clients can control the ratio of I to P frames using NV\_ENC\_RC\_PARAMS::lowDelayKeyFrameScale which is useful to avoid channel congestion in case I frame ends up generating high number of bits. Set NV\_ENC\_CONFIG\_H264/NV\_ENC\_CONFIG\_HEVC::enableFillerDataInsertion = 1 incase the bitrate needs to be strictly adhered to.

Variable bitrate (VBR): Variable bitrate is specified by setting rateControlMode to NV\_ENC\_PARAMS\_RC\_VBR. The encoder tries to conform to average bitrate of averageBitRate over the long term while not exceeding maxBitRate any time during the encoding. In this mode, averageBitRate must be specified. If maxBitRate isn't specified, NVENC will set it to an internally determined default value. It is recommended that the client specify both parameters maxBitRate and averageBitRate for better control.

Constant QP: This mode is specified by setting rateControlMode to NV\_ENC\_PARAMS\_RC\_CONSTQP. In this mode, the entire frame is encoded using QP specified in NV\_ENC\_RC\_PARAMS::constQP.

Target quality: This mode is specified by setting rateControlMode to VBR and desired target quality in targetQuality. The range of this target quality is 0 to 51(fractional values are also supported in Video Codec SDK 8.0 and above). In this mode, the encoder tries to maintain constant quality for each frame, by allowing the bitrate to vary subject to the bitrate parameter specified in maxBitRate. The resulting average bitrate can, therefore, vary significantly depending on the video content being encoded. If maxBitRate is not specified, the encoder will use as many bits as needed to achieve the target quality. However, if maxBitRate is set, it will form an upper bound on the actual bitrate. If maxBitRate is set too low in this mode, the bitrate may become constrained, resulting in the desired target quality possibly not being achieved.

See https://docs.nvidia.com/video-technologies/video-codec-

When determining the QP to use for encoding a frame, it is beneficial if NVENC knows the overall complexity of the frame to distribute the available bit budget in the most optimal manner. In some situations, multi-pass encoding may also help catch larger motion between frames. For this purpose, NVENC supports the following types of multi-pass frame encoding modes:

- 1-pass per frame encoding (NV ENC MULTI PASS DISABLED)
- 2-passes per frame, with first pass in quarter resolution and second pass in full resolution [NV ENC TWO PASS QUARTER RESOLUTION]
- 2-passes per frame, with both passes in full resolution (NV ENC TWO PASS FULL RESOLUTION).

In 1-pass rate control modes, NVENC estimates the required QP for the macroblock and immediately encodes the macroblock. In 2-pass rate control modes, NVENC estimates the complexity of the frame to be encoded and determines bit distribution across the frame in the first pass. In the second pass, NVENC encodes macroblocks in the frame using the distribution determined in the first pass. As a result, with 2-pass rate control modes, NVENC can distribute the bits more optimally within the frame and can reach closer to the

target bitrate, especially for CBR encoding. Note, however, that everything else being the same, performance of 2-pass rate control mode is lower than that of 1-pass rate control mode. The client application should choose an appropriate multi-pass rate control mode after evaluating various modes, as each of the modes has its own advantages and disadvantages. NV\_ENC\_TWO\_PASS\_FULL\_RESOLUTION generates better statistics for the second pass, whereas NV\_ENC\_TWO\_PASS\_QUARTER\_RESOLUTION results in larger motion vectors being caught and fed as hints to second pass.

See https://docs.nvidia.com/video-technologies/video-codec-sdk/pdf/NVENC\_VideoEncoder\_API\_ProgGuide.pdf at pp. 10-11.

28. On information and belief, the Accused Computer Products employ and provide a method comprising the step of calculating for each video-data item to be coded, a reference throughput as a function of the reference quantization value and transmitting the reference throughput to the coder, allowing the coder to code each video-data item so as to obtain video data at the predetermined quality, after decoding, as demonstrated below.

NVENC supports several rate control modes and provides control over various parameters related to the rate control algorithm via structure NV\_ENC\_INITIALIZE\_PARAMS::encodeConfig::rcParams. The rate control algorithm is implemented in NVENC firmware.

NVENC supports the following rate control modes:

Constant bitrate (CBR): Constant bitrate is specified by setting rateControlMode to NV\_ENC\_PARAMS\_RC\_CBR. In this mode, only averageBitRate is required and used as the target output bitrate by the rate control algorithm. Clients can control the ratio of I to P frames using NV\_ENC\_RC\_PARAMS::lowDelayKeyFrameScale which is useful to avoid channel congestion in case I frame ends up generating high number of bits. Set NV\_ENC\_CONFIG\_H264/NV\_ENC\_CONFIG\_HEVC::enableFillerDataInsertion = 1 incase the bitrate needs to be strictly adhered to.

Variable bitrate (VBR): Variable bitrate is specified by setting rateControlMode to NV\_ENC\_PARAMS\_RC\_VBR. The encoder tries to conform to average bitrate of averageBitRate over the long term while not exceeding maxBitRate any time during the encoding. In this mode, averageBitRate must be specified. If maxBitRate isn't specified, NVENC will set it to an internally determined default value. It is recommended that the client specify both parameters maxBitRate and averageBitRate for better control.

Constant QP: This mode is specified by setting rateControlMode to NV\_ENC\_PARAMS\_RC\_CONSTQP. In this mode, the entire frame is encoded using QP specified in NV\_ENC\_PARAMS::constQP.

Target quality: This mode is specified by setting rateControlMode to VBR and desired target quality in targetQuality. The range of this target quality is 0 to 51(fractional values are also supported in Video Codec SDK 8.0 and above). In this mode, the encoder tries to maintain constant quality for each frame, by allowing the bitrate to vary subject to the bitrate parameter specified in maxBitRate. The resulting average bitrate can, therefore, vary significantly depending on the video content being encoded. If maxBitRate is not specified, the encoder will use as many bits as needed to achieve the target quality. However, if maxBitRate is set, it will form an upper bound on the actual bitrate. If maxBitRate is set too low in this mode, the bitrate may become constrained, resulting in the desired target quality possibly not being achieved.

See https://docs.nvidia.com/video-technologies/video-codec-

When determining the QP to use for encoding a frame, it is beneficial if NVENC knows the overall complexity of the frame to distribute the available bit budget in the most optimal manner. In some situations, multi-pass encoding may also help catch larger motion between frames. For this purpose, NVENC supports the following types of multi-pass frame encoding modes:

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target bitrate, especially for CBR encoding. Note, however, that everything else being the same, performance of 2-pass rate control mode is lower than that of 1-pass rate control mode. The client application should choose an appropriate multi-pass rate control mode after evaluating various modes, as each of the modes has its own advantages and disadvantages.

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See https://docs.nvidia.com/video-technologies/video-codec-sdk/pdf/NVENC\_VideoEncoder\_API\_ProgGuide.pdf at pp. 10-11.

- 29. On information and belief, ASUS directly infringes at least claims 1 and 8 of the '167 patent, and is in violation of 35 U.S.C. § 271(a) by making, using, selling, and offering to sell the Accused Computer Products.
- 30. ASUS's direct infringement has damaged Burley and caused it to suffer and continue to suffer irreparable harm and damages.

#### **JURY DEMANDED**

31. Pursuant to Federal Rule of Civil Procedure 38(b), Burley hereby requests a trial by jury on all issues so triable.

### **PRAYER FOR RELIEF**

Burley respectfully requests this Court to enter judgment in Burley's favor and against ASUS as follows:

- a. finding that ASUS has infringed one or more claims of the '167 patent under 35 U.S.C. §§ 271(a);
- b. awarding Burley damages under 35 U.S.C. § 284, or otherwise permitted by law, including supplemental damages for any continued post-verdict infringement;
- c. awarding Burley pre-judgment and post-judgment interest on the damages award and costs;
- d. awarding cost of this action (including all disbursements) and attorney fees pursuant to 35 U.S.C. § 285, or as otherwise permitted by the law; and
- e. awarding such other costs and further relief that the Court determines to be just and equitable.

Dated: October 5, 2022 Respectfully submitted,

/s/ Zachary H. Ellis

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